Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**SOURCE connection centrally between indicator lines = 40 mils**

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**Top Material: Al**

**Backside Material: TiNiAg**

**GATE: .021” X .025”**

**Backside Potential: DRAIN**

**Mask Ref: GEN 5**

**APPROVED BY: DK DIE SIZE .087” X .121” DATE: 8/30/22**

**MFG: INT’L RECTIFIER THICKNESS .013” P/N: IRFC130**

**DG 10.1.2**

#### Rev B, 7/19/02